Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A method for programming a single-poly electrical programmable read only memory (EPROM) cell, said single-poly EPROM cell comprising a P-channel floating gate transistor on an isolated N-well of a P-type substrate, and an N-channel coupling device, wherein said P-channel floating gate transistor comprises P^+ drain, P^+ source, P channel defined between said P^+ drain and P^+ source, tunnel oxide on said P channel, and doped ploysilicon floating gate on said tunnel oxide, and wherein said N-channel coupling device comprises a polysilicon floating electrode that is electrically connected to said doped ploysilicon floating gate and is capacitively coupled to a control doped region formed in said P-type substrate, the method comprising:

grounding said P-type substrate;

grounding said N-well;

biasing said P^+ drain of said P-channel floating gate transistor to a negative voltage;

grounding or floating said P^+ source of said P-channel floating gate transistor; and

applying a positive voltage on said control doped region

so that said positive voltage being coupled to said P-doped ploysilicon floating gate, wherein said P channel of said P-channel floating gate transistor is in "OFF" state, and a depletion region and electron-hole pairs are created at a junction between said P^+ drain and said N well, and band-to-band tunneling (BTBT) induced hot electrons will inject into said doped ploysilicon floating gate by tunneling through said tunnel oxide.

[c2] 2.The method for programming a single-poly EPROM cell according to claim 1 wherein said positive voltage applied on said control doped region is Vcc.

[c3] 3.The method for programming a single-poly EPROM cell according to claim 2 wherein Vcc = +3.3V.

[c4] 4.The method for programming a single-poly EPROM cell according to claim 1 wherein said positive voltage applied on said control doped region is Vcc~2Vcc.

[c5] 5.The method for programming a single-poly EPROM cell according to claim 1 wherein said negative voltage is —Vcc.

[c6] 6.The method for programming a single-poly EPROM cell according to claim 1 wherein said negative voltage is —3.3V.

[c7] 7.The method for programming a single-poly EPROM cell according to claim 1 wherein a field oxide layer is disposed between said control doped region and said N well.

[c8] 8.The method for programming a single-poly EPROM cell according to claim 1 wherein shallow trench isolation (STI) is disposed between said control doped region and said N well.

[c9] 9.The method for programming a single-poly EPROM cell according to claim 1 wherein said polysilicon floating electrode of said N-channel coupling device is N-type doped polysilicon floating electrode.

[c10] 10.The method for programming a single-poly EPROM cell according to claim 1 wherein said tunnel oxide has a thickness of about 65Å.

[c11] 11.A method for programming a single-poly electrical programmable read only memory (EPROM) cell, said single-poly EPROM cell comprising a P-channel floating gate transistor on an isolated N-well of a P-type substrate, and an N-channel coupling device, wherein said P-channel floating gate transistor comprises P^+ drain, P^+ source, P channel defined between said P^+ drain and P^+ source, tunnel oxide on said P channel, and doped

ploysilicon floating gate on said tunnel oxide, and wherein said N-channel coupling device comprises a polysilicon floating electrode that is electrically connected to said doped ploysilicon floating gate and is capacitively coupled to a control doped region formed in said P-type substrate, wherein said N-well is isolated from said control doped region, the method comprising:
grounding said P-type substrate;
grounding said N-well;
applying a negative voltage of —Vcc to said P^+ drain of said P-channel floating gate transistor;
applying a parasitic BJT turn-on voltage to said P^+ source of said P-channel floating gate transistor; and
applying a positive voltage of +Vcc to said control doped region so that said positive voltage of +Vcc being coupled to said doped ploysilicon floating gate.

[c12] 12.The method for programming a single-poly EPROM cell according to claim 11 wherein said parasitic BJT turn-on voltage is a positive voltage that is adequate to turn on a parasitic bipolar junction transistor, wherein said P^+ source acts as an emitter, said P^+ drain acts as an collector, and said N well acts as a base.

[c13] 13.The method for programming a single-poly EPROM cell according to claim 12 wherein when said parasitic bipolar junction transistor is turned on, a large collector-

emitter current I_{CE} with abundant electrons flow will supply the electron hole pairs at said P^+ drain junction, thereby enhancing BTBT tunneling.

[c14] 14.The method for programming a single-poly EPROM cell according to claim 11 wherein said parasitic BJT turn-on voltage is about +0.7V.

[c15] 15.The method for programming a single-poly EPROM cell according to claim 11 wherein Vcc = +3.3V.

[c16] 16.The method for programming a single-poly EPROM cell according to claim 11 wherein said tunnel oxide has a thickness of about 65Å.